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3. Write The Verilog Program For Your Design (e.g.: Codefile1.v) Gedit Codefile1.v 4. Write The Verilog Test Bench Program For Your Design (e.g.: Codefile1_tb.v). Now, The Design Entry Using HDL Gets Finished. Gedit Codefile1_tb.v II. STEPS FOR SIMULATION: 1. Initially, Both Of Your Verilog Programs Have To Be Compiled 2. Feb 11th, 2024

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