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3 5 Class Textbooks And References Required Textbooks J. Bhasker, “A VHDL Synthesis Primer,” Second Edition, Star Galaxy Press, 1998. Supplementary Textbooks H. Bhatnagar, “Advanced ASIC Chip Synthesis 25th, 2024

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ASIC Physical Design (Standard Cell) (can Also Do Full Custom Layout) Floorplan Chip/Block. Place & Route. Std. Cells. Component-Level Verilog Netlist 27th, 2024

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Data Is Taken As Unsigned 16.0 Format And The Output Is Put In Unsigned 4.12 Format. The Whole Portion Of The Output Is

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