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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [Jan 18th, 2024

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Bode, Chu, Fano, Wheeler: Antenna Q And Match Bandwidth

Steve Stearns, K6OIK ARRL Pacificon Antenna Seminar, Santa Clara, CA October 11-13, 2013 R.C. Hansen And R.E. Collin, Small Antenna Handbook, Wiley, 2011, ISBN 0470890835 Mar 24th, 2024

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